PSoC™

PSoC® 4 ARM® Cortex™-M0+ CPU PSoC 4100S PSoC 4 CapSense PSoC 4100S PSoC 4

32 MCU

- 48 MHz ARM Cortex-M0+ CPU
- 64 KB
- SRAM 8 KB

- ADC
- 12 1 Msps SAR ADC
- 10 ADC
- DAC IDAC
-

- Boolean

1.71 V ~ 5.5 V

- 2.5 µA

- CapSense Sigma-Delta CSD SNR > 5:1
-
- SmartSense™

LCD

- GPIO LCD segment

- SCB I2C SPI UART

- 16 TCPWM
-
- Kill

36 GPIO

- 48 TQFP 40 QFN 32 QFN 35 WLCSP
- GPIO CapSense
-

PSoC Creator

- IDE
- API
- ARM

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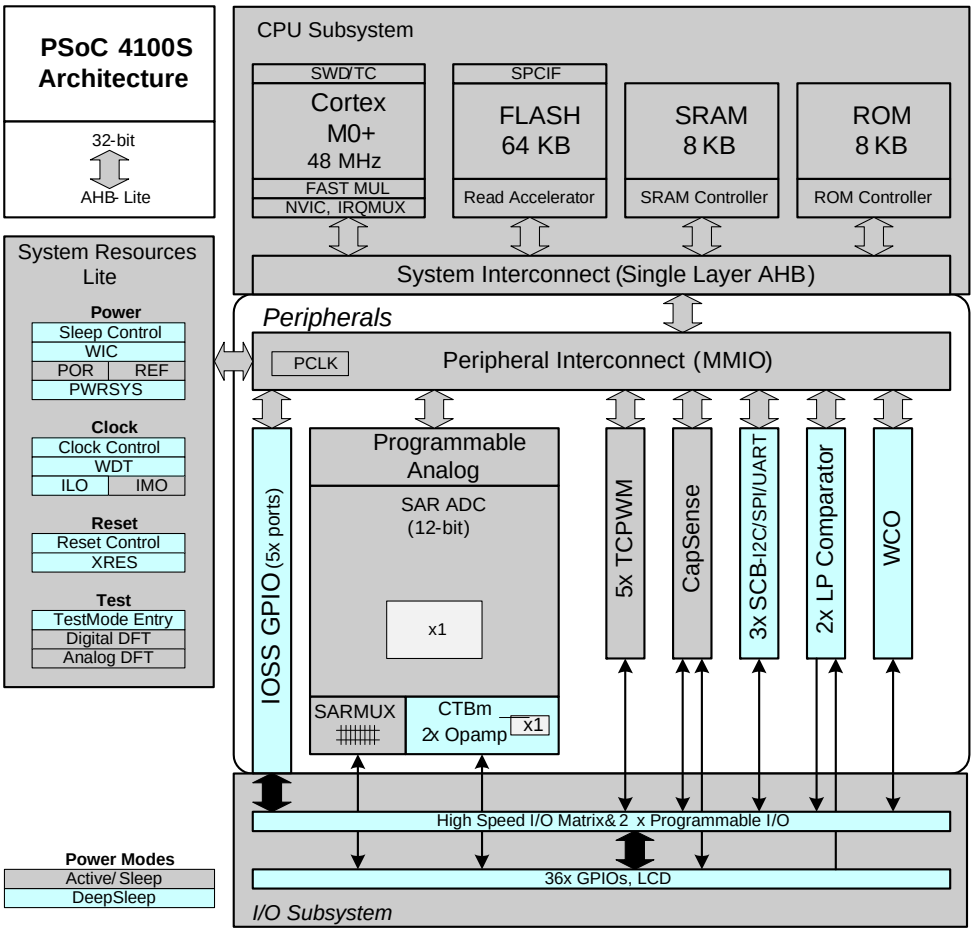

PSoC 4100S

ARM SWD DoC

PSoC Creator IDE PSoC 4100S SWD PSoC 4100S

4100S PSoC 4100S PSoC

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CPU

CPU

PSoC 4100S Cortex-M0+ CPU 32 MCU
16 CPU Thumb-2 8 NVIC WIC WIC
CPU SWD JTAG 2
PSoC 4100S

PSoC 4100S CPU 48 MHz WS 85% SRAM

SRAM

8 KB SRAM 48 MHz

SROM

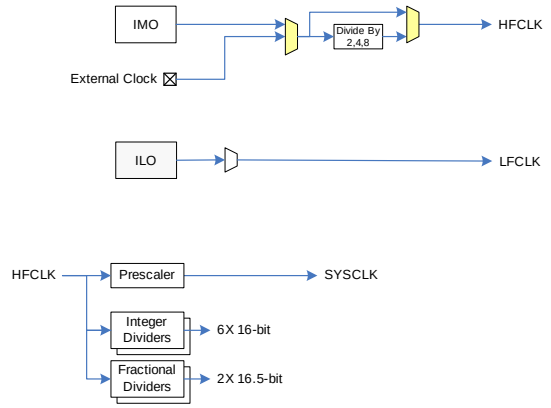
8 KB ROM

11 POR PSoC 4100S 1.8 V ±5% 1.8 V 5.5 V
PSoC 4100S
CPU CPU SRAM 35 µs

PSoC 4100S

PSoC 4100S IMO ILO 32 kHz WCO
UART

2. PSoC 4100S MCU



HFCLK 8 16 PSoC Creator

IMO

PSoC 4100S IMO IMO
24 MHz 4 MHz 24 MHz 48 MHz
IMO ±2%

ILO

ILO 40 kHz WDT IMO
ILO

WCO

PSoC 4100S
32 kHz

ILO

PSoC 4100S

XRES

XRES

12 SAR ADC

12 1 Msps SAR ADC 18 MHz 12 18

S/H SAR

SAR

SAR ADC 8

1 Msps

CPU

SAR ADC

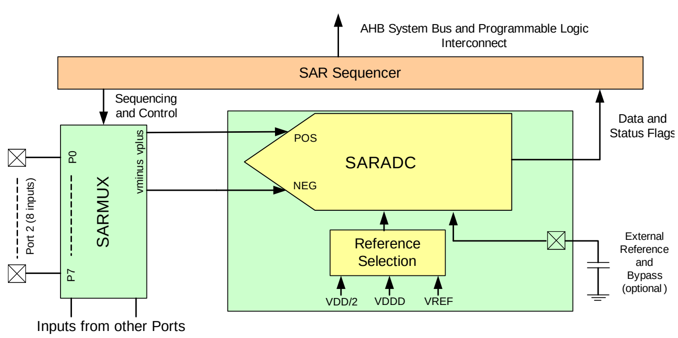
ADC

CPU

SAR 18 MHz

SAR 1.71 V 5.5 V

3. SAR ADC



CTB

PSoC 4100S

PGA

ADC

LPC

PSoC 4100S

LPC

DAC

PSoC 4100S IDAC

IDAC

PSoC 4100S

AMUX

IDAC

I/O

I/O PRGIO Smart I/O

LUT GPIO

Boolean PRGIO

/PWM TCPWM

TCPWM 16

I/O

PWM

PWM

Kill

FET PWM

PSoC 4100S TCPWM

SCB

PSoC 4100S SPI I2C

UART

I2C I2C

400 kbps

CPU

EZI2C PSoC

4100S

I2C

8 FIFO

CPU

CPU

I2C I2C

NXP I2C

UM10204

GPIO

I2C I/O

PSoC 4100S I2C

■ GPIO

I2C

UART 1 Mbps UART

LIN IrDA

ISO7816 UART

9

RX TX UART

8 FIFO CPU

SPI SPI Motorola SPI TI SSP

SPI National Microwire SPI

SPI FIFO

GPIO

PSoC 4000S 36 GPIO Â GPIO

■

Й PSoC 4100S 48 TQFP 40 QFN 32 QFN 36 CSP № Â GPIO Â

1.

48-TQFP		40-QFN		32-QFN		35-CSP	
28	P0.0	22	P0.0	17	P0.0	C3	P0.0
29	P0.1	23	P0.1	18	P0.1	A5	P0.1
30	P0.2	24	P0.2	19	P0.2	A4	P0.2
31	P0.3	25	P0.3	20	P0.3	A3	P0.3
32	P0.4	26	P0.4	21	P0.4	B3	P0.4
33	P0.5	27	P0.5	22	P0.5	A6	P0.5
34	P0.6	28	P0.6	23	P0.6	B4	P0.6
35	P0.7	29	P0.7	–	–	B5	P0.7
36	XRES	30	XRES	24	XRES	B6	XRES
37	VCCD	31	VCCD	25	VCCD	A7	VCCD
38	VSSD	DN	VSSD	26	VSSD	B7	VSS
39	VDDD	32	VDDD	–	–	C7	VDD
40	VDDA	33	VDDA	27	VDD	C7	VDD
41	VSSA	34	VSSA	28	VSSA	B7	VSS
42	P1.0	35	P1.0	29	P1.0	C4	P1.0
43	P1.1	36	P1.1	30	P1.1	C5	P1.1
44	P1.2	37	P1.2	31	P1.2	C6	P1.2
45	P1.3	38	P1.3	32	P1.3	D7	P1.3
46	P1.4	39	P1.4	–	–	D4	P1.4
47	P1.5	–	–	–	–	D5	P1.5
48	P1.6	–	–	–	–	D6	P1.6
1	P1.7/VREF	40	P1.7/VREF	1	P1.7/VREF	E7	P1.7/VREF
2	P2.0	1	P2.0	2	P2.0	–	–
3	P2.1	2	P2.1	3	P2.1	–	–
4	P2.2	3	P2.2	4	P2.2	D3	P2.2
5	P2.3	4	P2.3	5	P2.3	E4	P2.3
6	P2.4	5	P2.4			E5	P2.4
7	P2.5	6	P2.5	6	P2.5	E6	P2.5
8	P2.6	7	P2.6	7	P2.6	E3	P2.6
9	P2.7	8	P2.7	8	P2.7	E2	P2.7
10	VSSD	9	VSSD	–	–	–	–
12	P3.0	10	P3.0	9	P3.0	E1	P3.0
13	P3.1	11	P3.1	10	P3.1	D2	P3.1
14	P3.2	12	P3.2	11	P3.2	D1	P3.2
16	P3.3	13	P3.3	12	P3.3	C1	P3.3
17	P3.4	14	P3.4	–	–	C2	P3.4
18	P3.5	15	P3.5	–	–	–	–

1. ˆ ˜

48-TQFP		40-QFN		32-QFN		35-CSP	
	٦		٦		٦		٦
19	P3.6	16	P3.6	–	–	–	–
20	P3.7	17	P3.7	–	–	–	–
21	VDDD	–	–	–	–	–	–
22	P4.0	18	P4.0	13	P4.0	B1	P4.0
23	P4.1	19	P4.1	14	P4.1	B2	P4.1
24	P4.2	20	P4.2	15	P4.2	A2	P4.2
25	P4.3	21	P4.3	16	P4.3	A1	P4.3

ˈ خي 48 TQFP 11 à 15 à 26 ˇ 27 ˆ NC˜ Â

Ø ˇ Ий ˈ

VDDDˈ №

VDDAˈ №

VSSD à VSSAˈ № ч ˇ № شم Â

VCCDˈ ل ˆ 1.8 V ± 5%˜

I/O LCD CapSense PRGIO Smart I/O

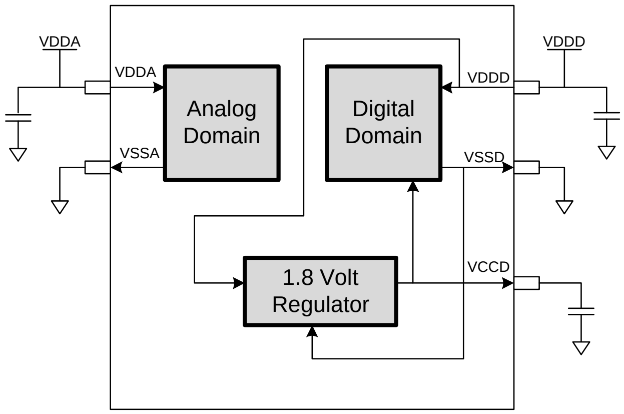
/		I/O	1	2	3	1	2
P0.0	lpcomp.in_p[0]	–	–	scb[2].uart_cts:0	tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]	–	–	scb[2].uart_rts:0	tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]	–	–	–	–	–	scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]	–	–	–	–	–	scb[2].spi_select0
P0.4	wco.wco_in	–	–	scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out	–	–	scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	–	–	srss.ext_clk	scb[1].uart_cts:0	scb[2].uart_tx:1	–	scb[1].spi_clk:1
P0.7	–	–	tcpwm.line[0]:2	scb[1].uart_rts:0	–	–	scb[1].spi_select0:1
P1.0	ctb0_oa0+	–	tcpwm.line[2]:1	scb[0].uart_rx:1	–	scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-	–	tcpwm.line_compl[2]:1	scb[0].uart_tx:1	–	scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out	–	tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	ctb0_oa1_out	–	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.4	ctb0_oa1-	–	–	–	–	–	scb[0].spi_select1:1
P1.5	ctb0_oa1+	–	–	–	–	–	scb[0].spi_select2:1
P1.6	ctb0_oa0+	–	–	–	–	–	scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1	–	–	–	–	–	scb[2].spi_clk
P2.0	sarmux[0]	prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	prgio[0].io[1]	tcpwm.line_compl[4]:0	–	tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	prgio[0].io[2]	–	–	–	–	scb[1].spi_clk:2

P2.3	sarmux[3]	prgio[0].io[3]	–	–	–	–	scb[1].spi_select0:2
P2.4	sarmux[4]	prgio[0].io[4]	tcpwm.line[0]:1	–	–	–	scb[1].spi_select1:1
P2.5	sarmux[5]	prgio[0].io[5]	tcpwm.line_compl[0]:1	–	–	–	scb[1].spi_select2:1
P2.6	sarmux[6]	prgio[0].io[6]	tcpwm.line[1]:1	–	–	–	scb[1].spi_select3:1
P2.7	sarmux[7]	prgio[0].io[7]	tcpwm.line_compl[1]:1	–	–	lpcomp.comp[0]:1	scb[2].spi_mosi
P3.0	–	prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1	–	scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1	–	prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1	–	scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2	–	prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1	–	cpuss.swd_data	scb[1].spi_clk:0
P3.3	–	prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1	–	cpuss.swd_clk	scb[1].spi_select0:0
P3.4	–	prgio[1].io[4]	tcpwm.line[2]:0	–	tcpwm.tr_in[6]	–	scb[1].spi_select1:0
P3.5	–	prgio[1].io[5]	tcpwm.line_compl[2]:0	–	–	–	scb[1].spi_select2:0
P3.6	–	prgio[1].io[6]	tcpwm.line[3]:0	–	–	–	scb[1].spi_select3:0
P3.7	–	prgio[1].io[7]	tcpwm.line_compl[3]:0	–	–	lpcomp.comp[1]:1	scb[2].spi_miso
P4.0	csd.vref_ext	–	–	scb[0].uart_rx:0	–	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads	–	–	scb[0].uart_tx:0	–	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad	–	–	scb[0].uart_cts:0	–	lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank	–	–	scb[0].uart_rts:0	–	lpcomp.comp[1]:0	scb[0].spi_select0:0

PSoC 4100S

V_{DD}

4.



1 1.8 V 5.5 V
2 1.8 V

5. 1.8 V 5.5 V

±5% 1.71 1.89 V

1 1.8 V 5.5 V

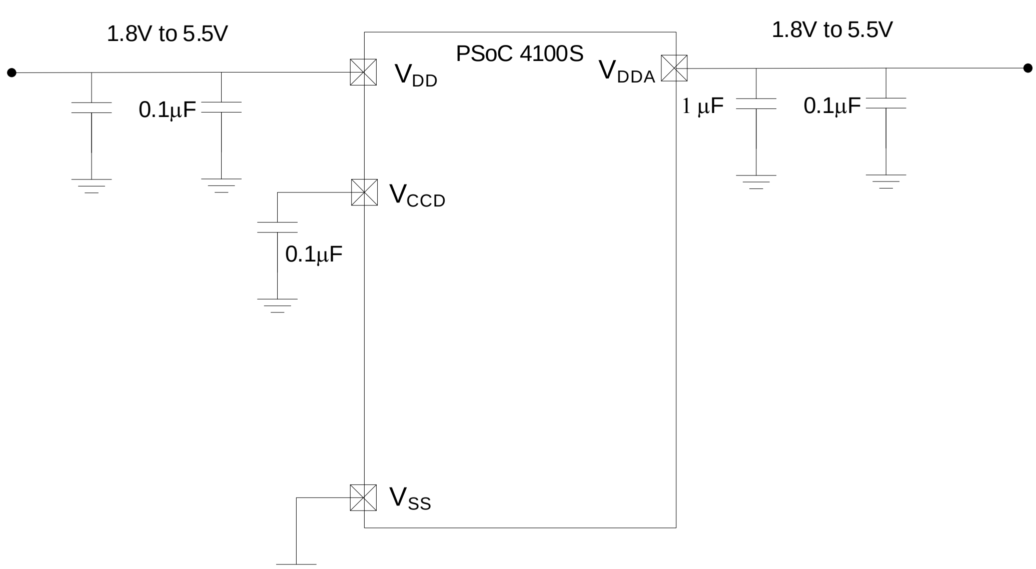
PSoC 4100S 1.8 5.5 V 3.5 V 1.8 V PSoC 4100S V_{CCD} VCCD 0.1 µF X5R

2 1.8 V ± 5%

PSoC 4100S 1.71 V 1.89 V VDD VCCD

VDDD 1 µF 0.1 µF PCB

Power supply bypass connections example



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PSoC 4100S Ƭ ˥ Â Ŧ ' Â ˓ PSoC Creator Â PSoC Creator à PSoC Creator Â

˓ PSoC IC خي ᵒᵒ Ӡ ˥ Ƭ ‸ ˜ Â ˇ ἰ ˝ à API à ˥ Ƭ ΰ̈ / Â

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2. [1]

ID							
SID1	V_{DDD_ABS}	V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	V_{SS}	–0.5	–	1.95	V	–
SID3	V_{GPIO_ABS}	GPIO	–0.5	–	V_{DD}+0.5	V	–
SID4	I_{GPIO_ABS}	GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO $V_{IH} > V_{DDD}$ $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	
BID44	ESD_HBM	—	2200	–	–	V	–
BID45	ESD_CDM	—	500	–	–	V	–
BID46	LU		–140	–	140	mA	–

–40 °C ≤ T_A ≤ 85 °C T_J ≤ 100 °C 1.71 V ~ 5.5 V

3.

V_{DD} = 3.3 V = 25 °C

ID#							
SID53	V_{DD}		1.8	–	5.5	V	
SID255	V_{DD}	$V_{CCD} = V_{DDD} = V_{DDA}$	1.71	–	1.89	V	
SID54	V_{CCD}		–	1.8	–	V	–
SID55	C_{EFC}		–	0.1	–	µF	X5R
SID56	C_{EXC}		–	1	–	µF	X5R
Ток		**V_{DD} = 1.8 V ~ 5.5 V 25 °C VDD = 3.3 V**					
SID10	I_{DD5}	6 MHz CPU	–	2	–	mA	–
SID16	I_{DD8}	24 MHz CPU	–	5.6	–	mA	–
SID19	I_{DD11}	48 MHz CPU	–	10.4	–	mA	–
Ток		**VDDD = 1.8 V ~ 5.5 V**					
SID22	IDD17	I^2C WDT	–	1.1	–	mA	6 MHz
SID25	IDD20	I^2C WDT	–	3.1	–	mA	12 MHz
Ток		**V_{DDD} = 1.71 V ~ 1.89 V**					

1. JEDEC JESD22-A103 — 150°C

3.

V_{DD} = 3.3 V = 25 °C

ID#							
SID28	IDD23	I^2C WDT	–	1.1	–	mA	6 MHz
SID28A	IDD23A	I^2C WDT	–	3.1	–	mA	12 MHz
V_{DD} = 1.8 V ~ 3.6 V							
SID31	I_{DD26}	I^2C WDT	–	2.5	–	µA	–
V_{DD} = 3.6 V ~ 5.5 V							
SID34	I_{DD29}	I^2C WDT	–	2.5	–	µA	–
V_{DD} = V_{CCD} = 1.71 V ~ 1.89 V							
SID37	I_{DD32}	I^2C WDT	–	2.5	–	µA	–
XRES							
SID307	I_{DD_XR}	XRES	–	2	5	mA	–

4.

ID							/
SID48	F_{CPU}	CPU	DC	–	48	MHz	1.71 ≤ V_{DD} ≤ 5.5
SID49[3]	T_{SLEEP}		–	0	–	µs	
SID50[3]	$T_{DEEPSLEEP}$		–	35	–	µs	

2.

GPIO

5. GPIO

ID							
SID57	V_{IH}[3]		0.7 × V_{DDD}	–	–	V	CMOS
SID58	V_{IL}		–	–	0.3 × V_{DDD}		CMOS
SID241	V_{IH}[3]	LVTTL	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[3]	LVTTL	2.0	–	–		–
SID244	V_{IL}	LVTTL	–	–	0.8		–
SID59	V_{OH}		V_{DDD} – 0.6	–	–		V_{DDD} = 3 V I_{OH} = 4 mA
SID60	V_{OH}		V_{DDD} – 0.5	–	–		V_{DDD} = 1.8 V I_{OH} = 1 mA
SID61	V_{OL}		–	–	0.6		V_{DDD} = 1.8 V I_{OL} = 4 mA
SID62	V_{OL}		–	–	0.6		V_{DDD} = 3 V I_{OL} = 10 mA
SID62A	V_{OL}		–	–	0.4		V_{DDD} = 3 V I_{OL} = 3 mA
SID63	R_{PULLUP}		3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$		3.5	5.6	8.5		–
SID65	I_{IL}		–	–	2	nA	25 °C V_{DDD} = 3.0 V
SID66	C_{IN}		–	–	7	pF	–
SID67[4]	V_{HYSTTL}	LVTTL	25	40	–	mV	V_{DDD} ≥ 2.7 V
SID68[4]	$V_{HYSCMOS}$	CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[4]	$V_{HYSCMOS5V5}$	CMOS	200	–	–		VDD < 4.5 V
SID69[4]	I_{DIODE}		–	–	100	µA	–
SID69A[4]	I_{TOT_GPIO}		–	–	200	mA	–

6. GPIO

ID							
SID70	T_{RISEF}		2	–	12	ns	3.3 V V_{DDD} Cload = 25 pF
SID71	T_{FALLF}		2	–	12		V_{DDD} = 3.3 V Cload = 25 pF
SID72	T_{RISES}		10	–	60	–	V_{DDD} = 3.3 V Cload = 25 pF
SID73	T_{FALLS}		10	–	60	–	V_{DDD} = 3.3 V Cload = 25 pF

3. V_{IH} V_{DDD} + 0.2 V
4.

SID74	$F_{GPIOUT1}$	GPIO 3.3 V ≤ V_{DDD} ≤ 5.5 V	–	–	33	MHz	90/10%	Cload = 25 pF

XRES

9. CTBm

ID							
	I_{DD}						
SID269	I_{DD_HI}	=	–	1100	1850	µA	–
SID270	I_{DD_MED}	=	–	550	950		–
SID271	I_{DD_LOW}	=	–	150	350		–
	G_{BW}	= 20 pF 0.1 mA V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	=	6	–	–	MHz	0.2 V ~ V_{DDA}-0.2 V
SID273	G_{BW_MED}	=	3	–	–		0.2 V ~ V_{DDA}-0.2 V
SID274	G_{BW_LO}	=	–	1	–		0.2 V ~ V_{DDA}-0.2 V
	I_{OUT_MAX}	V_{DDA} = 2.7 V = 500 mV					
SID275	$I_{OUT\_MAX\_HI}$	=	10	–	–	mA	0.5 V ~ V_{DDA}-0.5 V
SID276	$I_{OUT\_MAX\_MID}$	=	10	–	–		0.5 V ~ V_{DDA}-0.5 V
SID277	$I_{OUT\_MAX\_LO}$	=	–	5	–		0.5 V ~ V_{DDA}-0.5 V
	I_{OUT}	V_{DDA} = 1.71 V = 500 mV					
SID278	$I_{OUT\_MAX\_HI}$	=	4	–	–	mA	0.5 V ~ V_{DDA}-0.5 V
SID279	$I_{OUT\_MAX\_MID}$	=	4	–	–		0.5 V ~ V_{DDA}-0.5 V
SID280	$I_{OUT\_MAX\_LO}$	=	–	2	–		0.5 V ~ V_{DDA}-0.5 V
	I_{DD_Int}						
SID269_I	$I_{DD\_HI\_Int}$	=	–	1500	1700	µA	–
SID270_I	$I_{DD\_MED\_Int}$	=	–	700	900		–
SID271_I	$I_{DD\_LOW\_Int}$	=	–	–	–		–
	G_{BW}	V_{DDA} = 2.7 V	–	–	–		–
SID272_I	$G_{BW\_HI\_Int}$	=	8	–	–	MHz	0.25 V ~ V_{DDA}-0.25 V

9. CTBm

ID							
SID281	V_{IN}	V_{DDA} = 2.7 V	-0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	V_{DDA} = 2.7 V	-0.05	–	V_{DDA}-0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	= Iload = 10 mA	0.5	–	V_{DDA} -0.5	V	–
SID284	V_{OUT_2}	= Iload = 1 mA	0.2	–	V_{DDA}-0.2		–
SID285	V_{OUT_3}	= Iload = 1 mA	0.2	–	V_{DDA}-0.2		–
SID286	V_{OUT_4}	= Iload = 0.1 mA	0.2	–	V_{DDA}-0.2		–
SID288	V_{OS_TR}		–1.0	±0.5	1.0	mV	0 V ~ V_{DDA}-0.2 V
SID288A	V_{OS_TR}		–	±1	–		0 V ~ V_{DDA}-0.2 V
SID288B	V_{OS_TR}		–	±2	–		0 V ~ V_{DDA}-0.2 V
SID290	$V_{OS\_DR\_TR}$		–10	±3	10	µV/C	
SID290A	$V_{OS\_DR\_TR}$		–	±10	–	µV/C	
SID290B	$V_{OS\_DR\_TR}$		–	±10	–		
SID291	CMRR		70	80	–	dB	0 V ~ V_{DDA}-0.2 V 0.2 V ~ V_{DDA}-0.2 V
SID292	PSRR	1 kHz 10 mV	70	85	–		V_{DDD} = 3.6 V 0.2 V ~ V_{DDA}-0.2 V
SID294	VN2	= 1 kHz	–	72	–	nV/rtHz	3
SID295	VN3	= 10 kHz	–	28	–		0.2 V ~ V_{DDA}-0.2 V
SID296	VN4	= 100 kHz	–	15	–		0.2 V ~ V_{DDA}-0.2 V
SID297	C_{LOAD}	50 pF	–	–	125	pF	–

9. CTBm

ID							
SID298	SLEW_RATE	Cload = 50 pF = V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	RC	–	–	25	µs	–
SID299A	OL_GAIN		–	90	–	dB	
	COMP_MODE	50 mV $T_{rise} = T_{fall}$					
SID300	TPD1	=	–	150	–	ns	0.2 V ~ V_{DDA}-0.2 V
SID301	TPD2	=	–	500	–		0.2 V ~ V_{DDA}-0.2 V
SID302	TPD3	=	–	2500	–		0.2 V ~ V_{DDA}-0.2 V
SID303	VHYST_OP		–	10	–	mV	–
SID304	WUP_CTB		–	–	25	µs	–
		2 1 GBW					
SID_DS_1	$I_{DD\_HI\_M1}$	1	–	1400	–	µA	25°C
SID_DS_2	$I_{DD\_MED\_M1}$	1	–	700	–		25°C
SID_DS_3	$I_{DD\_LOW\_M1}$	1	–	200	–		25°C
SID_DS_4	$I_{DD\_HI\_M2}$	2	–	120	–		25°C
SID_DS_5	$I_{DD\_MED\_M2}$	2	–	60	–		25°C
SID_DS_6	$I_{DD\_LOW\_M2}$	2	–	15	–		25°C

9. CTBm

ID							
SID_DS_7	$G_{BW\_HI\_M1}$	1	–	4	–	MHz	20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	1	–	2	–		20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_9	$G_{BW\_LOW\_M!}$	1	–	0.5	–		20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	2	–	0.5	–		20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	2	–	0.2	–		20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	2	–	0.1	–		20 pF 0.2 V ~ V_{DDA}-0.2 V
SID_DS_13	$V_{OS\_HI\_M1}$	1	–	5	–	mV	25°C 0.2 V ~ V_{DDA}-0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	1	–	5	–		25°C 0.2 V ~ V_{DDA}-0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	1	–	5	–		25°C 0.2 V ~ V_{DDA}-0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	2	–	5	–		25°C 0.2 V ~ V_{DDA}-0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	2	–	5	–		25°C 0.2 V ~ V_{DDA}-0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	2	–	5	–		25°C 0.2 V ~ V_{DDA}-0.2 V

9. CTBm

ID							
SID_DS_19	$I_{OUT\_HI\_M!}$	1	–	10	–	mA	0.5 V ~ V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	1	–	10	–		0.5 V ~ V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	1	–	4	–		0.5 V ~ V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	2	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	2	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	2	–	0.5	–		

10.

ID							
SID84	$V_{OFFSET1}$		–	–	±10	mV	
SID85	$V_{OFFSET2}$		–	–	±4		
SID86	V_{HYST}		–	10	35		
SID87	V_{ICM1}		0	–	VDDD –0.1	V	1 2
SID247	V_{ICM2}		0	–	V_{DDD}		
SID247A	V_{ICM3}		0	–	V_{DDD} – 1.15		V_{DDD} ≥ 2.2 V –40 °C
SID88	C_{MRR}		50	–	–	dB	V_{DDD} ≥ 2.7 V
SID88A	C_{MRR}		42	–	–		V_{DDD} ≤ 2.7 V
SID89	I_{CMP1}		–	–	400	µA	
SID248	I_{CMP2}		–	–	100		
SID259	I_{CMP3}		–	–	6		V_{DDD} ≥ 2.2 V –40 °C
SID90	Z_{CMP}		35	–	–	MΩ	

6.

12.

ID							
SID93	TSENSACC		–5	±1	5	°C	–40 ~ +85 °C

13. SAR ADC

ID							
SAR ADC							
SID94	A_RES		–	–	12		
SID95	A_CHNLS_S		–	–	8		8
SID96	A-CHNKS_D		–	–	4		I/O
SID97	A-MONO		–	–	–		
SID98	A_GAINERR		–	–	±0.1	%	
SID99	A_OFFSET		–	–	2	mV	1 V
SID100	A_ISAR		–	–	1	mA	
SID101	A_VINS		V_{SS}	–	V_{DDA}	V	
SID102	A_VIND		V_{SS}	–	V_{DDA}	V	
SID103	A_INRES		–	–	2.2	KΩ	
SID104	A_INCAP		–	–	10	pF	
SID260	VREFSAR	SAR	–	–	TBD	V	
SAR ADC							
SID106	A_PSRR		70	–	–	dB	
SID107	A_CMRR		66	–	–	dB	1 V
SID108	A_SAMP		–	–	1	Msps	
SID109	A_SNR	SINAD	65	–	–	dB	F_{IN} = 10 kHz
SID110	A_BW		–	–	A_samp/2	kHz	
SID111	A_INL	V_{DD} = 1.71~ 5.5 V 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V~ V_{DD}
SID111A	A_INL	V_{DDD} = 1.71 V ~ 3.6 V 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V ~ V_{DD}
SID111B	A_INL	V_{DD} = 1.71 V ~ 5.5 V 500 Ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V~ V_{DD}
SID112	A_DNL	V_{DD} = 1.71 V ~ 5.5 V 1 Msps	–1	_	2.2	LSB	V_{REF} = 1 V ~ V_{DD}
SID112A	A_DNL	V_{DD} = 1.71 V ~ 3.6 V 1 Msps	–1	_	2	LSB	V_{REF} = 1.71 V ~ V_{DD}
SID112B	A_DNL	V_{DD} = 1.71 V ~ 5.5 V 500 Ksps	–1	_	2.2	LSB	V_{REF} = 1 V ~ V_{DD}
SID113	A_THD		–	–	–65	dB	Fin = 10 kHz
SID261	Fsarintref	SAR	–	–	100	ksps	12

14. CSD IDAC

ID						
SYS.PER#3	VDD_RIPPLE	10 MHz	–	–	±50	V_{DD} > 2 V T_A= 25 °C = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	10 MHz	–	–	±25	V_{DD} > 1.75 V T_A = 25 °C C_P < 20 pF ≥ 0.4 pF
SID.CSD.BLK	ICSD		–	–	1700	IDAC
SID.CSD#15	VREF	CSD	0.6	1.2	V_{DDA} - 0.6	V_{DDA} - 0.06 4.4
SID.CSD#15A	VREF_EXT	CSD	0.6		V_{DDA} - 0.6	V_{DDA} - 0.06 4.4
SID.CSD#16	IDAC1IDD	IDAC1	–	–	1500	
SID.CSD#17	IDAC2IDD	IDAC2	–	–	1500	
SID308	VCSD		1.71	–	5.5	1.8 V ±5% 1.8 V ~ 5.5 V
SID308A	VCOMPIDAC	IDAC	0.6	–	V_{DDA} - 0.6	V_{DDA} - 0.06 4.4
SID309	IDAC1DNL	DNL	–1	–	1	
SID310	IDAC1INL	INL	–3	–	3	
SID311	IDAC2DNL	DNL	–1	–	1	
SID312	IDAC2INL	INL	–3	–	3	
SID313	SNR		5	–	–	= 5 pF ~ 200 pF = 0.1 pF V_{DDA} > 2 V
SID314	IDAC1CRT1	IDAC1	4.2	–	5.2	LSB = 37.5 nA
SID314A	IDAC1CRT2	IDAC1	34	–	41	LSB = 300 nA
SID314B	IDAC1CRT3	IDAC1	275	–	330	LSB = 2.4 µA
SID314C	IDAC1CRT12	2X IDAC1	8	–	10.5	LSB = 37.5 nA 2X
SID314D	IDAC1CRT22	2X IDAC1	69	–	82	LSB = 300 nA 2X
SID314E	IDAC1CRT32	2X IDAC1	540	–	660	LSB = 2.4 nA 2X
SID315	IDAC2CRT1	IDAC2	4.2	–	5.2	LSB = 37.5 nA
SID315A	IDAC2CRT2	IDAC2	34	–	41	LSB = 300 nA
SID315B	IDAC2CRT3	IDAC2	275	–	330	LSB = 2.4 µA
SID315C	IDAC2CRT12	IDAC2 2X	8	–	10.5	LSB = 37.5 nA 2X

14. CSD IDAC

ID						
SID315D	IDAC2CRT22	IDAC2 7 2X	69	–	82	LSB = 300 nA 2X
SID315E	IDAC2CRT32	IDAC2 7 2X	540	–	660	LSB = 2.4 µA 2X
SID315F	IDAC3CRT13	IDAC 8	8	–	10.5	LSB = 37.5 nA
SID315G	IDAC3CRT23	IDAC 8	69	–	82	LSB = 300 nA
SID315H	IDAC3CRT33	IDAC 8	540	–	660	LSB = 2.4 µA
SID320	IDACOFFSET		–	–	1	
SID321	IDACGAIN		–	–	±10	
SID322	IDACMISMATCH1	IDAC1 IDAC2	–	–	9.2	LSB = 37.5 nA
SID322A	IDACMISMATCH2	IDAC1 IDAC2	–	–	4.6	LSB = 300 nA
SID322B	IDACMISMATCH3	IDAC1 IDAC2	–	–	2.3	LSB = 2.4 µA
SID323	IDACSET8	8 IDAC 0.5 LSB	–	–	10	
SID324	IDACSET7	7 IDAC 0.5 LSB	–	–	10	
SID325	CMOD		–	2.2	–	5 V X7R NP0

15. 10 CapSense ADC

ID							
SIDA94	A_RES		–	–	10		
SIDA95	A_CHNLS_S		–	–	16		AMUX
SIDA97	A-MONO		–	–	–		
SIDA98	A_GAINERR		–	–	TBD	%	
SIDA99	A_OFFSET		–	–	TBD	mV	
SIDA100	A_ISAR		–	–	TBD	mA	
SIDA101	A_VINS		VSSA	–	VDDA	V	
SIDA103	A_INRES		–	2.2	–	KΩ	
SIDA104	A_INCAP		–	20	–	pF	
SIDA106	A_PSRR		TBD	–	–	dB	
SIDA107	A_TACQ		–	1	–	µs	
SIDA108	A_CONV8	Fhclk/(2^(N+2)) 8 48 MHz	–	–	21.3	µs	44.8 ksps
SIDA108A	A_CONV10	Fhclk/(2^(N+2)) 10 48 MHz	–	–	85.3	µs	11.6 ksps
SIDA109	A_SND	SINAD	TBD	–	–	dB	

15. 10 CapSense ADC

ID							
SIDA110	A_BW	9	–	–	22.4	KHz	8
SIDA111	A_INL	1 ksps	–	–	2	LSB	VREF = 2.4 V
SIDA112	A_DNL	1 ksps	–	–	1	LSB	

/ / TCPWM

16. TCPWM

ID							
SID.TCPWM.1	ITCPWM1	3 MHz	–	–	45	µA	TCPWM
SID.TCPWM.2	ITCPWM2	12 MHz	–	–	155		TCPWM
SID.TCPWM.2A	ITCPWM3	48 MHz	–	–	650		TCPWM
SID.TCPWM.3	$TCPWM_{FREQ}$		–	–	Fc	MHz	Fc max = CLK_SYS = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$		2/Fc	–	–	ns	[7]
SID.TCPWM.5	$TPWM_{EXT}$		2/Fc	–	–		CC
SID.TCPWM.5A	TC_{RES}		1/Fc	–	–		
SID.TCPWM.5B	PWM_{RES}	PWM	1/Fc	–	–		PWM
SID.TCPWM.5C	Q_{RES}		1/Fc	–	–		

I^2C

17. I^2C [8]

ID							
SID149	I_{I2C1}	100 KHz	–	–	50	µA	–
SID150	I_{I2C2}	400 KHz	–	–	135		–
SID151	I_{I2C3}	1 Mbps	–	–	310		–
SID152	I_{I2C4}		–	–	1.4		

18. I^2C [8]

ID							
SID153	F_{I2C1}		–	–	1	Msps	–

7. Stop Start Reload Count Capture Kill
8.

19. SPI [9]

ID							
SID163	ISPI1	1 Mbps	–	–	360	µA	–
SID164	ISPI2	4 Mbps	–	–	560		–
SID165	ISPI3	8 Mbps	–	–	600		–

20. SPI [9]

ID							
SID166	FSPI	SPI 6X	–	–	8	MHz	SID166
SPI							
SID167	TDMO	SClock MOSI	–	–	15	ns	–
SID168	TDSI	SClock MISO	20	–	–		MISO
SID169	THMO	MOSI	0	–	–		
SPI							
SID170	TDMI	SClock MOSI	40	–	–	ns	–
SID171	TDSO	SClock MISO	–	–	42 + 3*Tcpu		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	Sclock MISO	–	–	48		–
SID172	THSO	MISO	0	–	–		–
SID172A	TSSELSSCK	SSEL SCK	–	–	100	ns	–

21. UART [9]

ID							
SID160	I_{UART1}	100 Kbits/s	–	–	55	µA	–
SID161	I_{UART2}	1000 Kbits/s	–	–	312	µA	–

22. UART [9]

ID							
SID162	F_{UART}		–	–	1	Mbps	–

23. LCD

[9]

ID							
SID154	I_{LCDLOW}		–	5	–	µA	16 × 4 Segment = 50 Hz
SID155	C_{LCDCAP}	LCD Segment/Common	–	500	5000	pF	–
SID156	LCD_{OFFSET}		–	20	–	mV	–
SID157	I_{LCDOP1}	LCD Vbias = 5 V	–	2	–	mA	32 × 4 50 Hz 25 °C
SID158	I_{LCDOP2}	LCD Vbias = 3.3 V	–	2	–		32 × 4 50 Hz 25 °C

24. LCD

[9]

ID							
SID159	F_{LCD}	LCD	10	50	150	Hz	–

9.

25.

ID							
SID173	V_{PE}		1.71	–	5.5	V	–

26.

ID							
SID174	$T_{ROWWRITE}$[10]		–	–	20	ms	= 128
SID175	$T_{ROWERASE}$[10]		–	–	13		–
SID176	$T_{ROWPROGRAM}$[10]		–	–	7		–
SID178	$T_{BULKERASE}$[10]	64 KB	–	–	35		–
SID180[11]	$T_{DEVPROG}$[10]		–	–	7		–
SID181[11]	F_{END}		100 K	–	–		–
SID182[11]	F_{RET}	10 / $T_A \leq 55$ °C	20	–	–		–
SID182A[11]	–	/ $T_A \leq 85$ °C	10	–	–		–
SID256	TWS48	48 MHz	2	–	–		CPU
SID257	TWS24	24 MHz	1	–	–		CPU

POR

27. PRES

ID							
SID.CLK#6	SR_POWER_UP		1	–	67	V/ms	
SID185[11]	$V_{RISEIPOR}$		0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$		0.70	–	1.4		–

28. V_{CCD} BOD

ID							
SID190[11]	$V_{FALLPPOR}$	BOD	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD	1.11	–	1.5		–

10. 20 XRES CPU
11.

SWD

29. SWD

ID							
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ CPU 1/3
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ CPU 1/3
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T		–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

30. IMO

ID							
SID218	I_{IMO1}	48 MHz IMO	–	–	250	µA	–
SID219	I_{IMO2}	24 MHz IMO	–	–	180	µA	–

31. IMO

ID							
SID223	$F_{IMOTOL1}$	24 à 32 48 MHz	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	24 MHz	–	145	–	ps	–

32. ILO

ID							
SID231[12]	I_{ILO1}	ILO	–	0.3	1.05	µA	–

33. ILO

ID							
SID234[12]	$T_{STARTILO1}$	ILO	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO	20	40	80	kHz	–

12. Â

34. WCO

ID							
SID398	FWCO		–	32.768	–	kHz	
SID399	FTOL		–	50	250	ppm	20 ppm
SID400	ESR		–	50	–	kΩ	
SID401	PD		–	–	1	µW	
SID402	TSTART		–	–	500	ms	
SID403	CL		6	–	12.5	pF	
SID404	C0		–	1.35	–	pF	
SID405	IWCO1		–	–	8	uA	
SID406	IWCO2		–	–	1	uA	

35.

ID							
SID305[13]	ExtClkFreq		0	–	48	MHz	–
SID306[13]	ExtClkDuty	$V_{DD/2}$	45	–	55	%	–

36.

ID							
SID262[13]	$T_{CLKSWITCH}$		3	–	4		–

37. PRGIO

ID							
SID252	PRG_BYPASS	PRGIO	–	–	1.6	ns	PRGIO Smart I/O

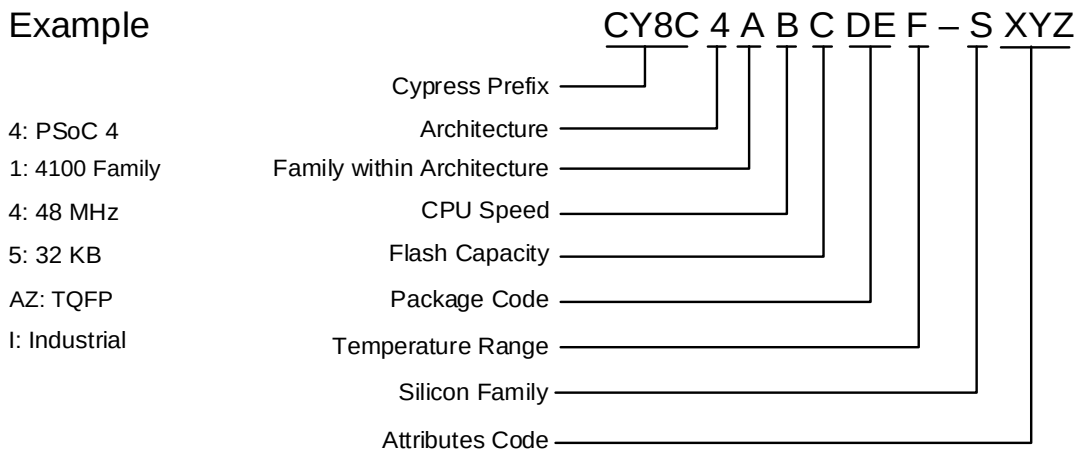
13.

Й PSoC 4100S Â

	MPN	CPU MHz	KB	SRAM KB	CTBm	CSD	12 SAR ADC	ADC	TCPWM	SCB	I/O I/O	GPIO	35-WLCSP	32-QFN	40-QFN	48-TQFP
4124	CY8C4124FNI-S403	24	16	4	2	0	0	–	2	5	2	8	31	X	–	–	–
	CY8C4124FNI-S413	24	16	4	2	1	0	–	2	5	2	16	31	X	–	–	–
	CY8C4124LQI-S412	24	16	4	2	1	0	–	2	5	2	16	27	–	X	–	–
	CY8C4124LQI-S413	24	16	4	2	1	0	–	2	5	2	16	34	–	–	X	–
	CY8C4124AZI-S413	24	16	4	2	1	0	–	2	5	2	16	36	–	–	–	X
	CY8C4124FNI-S433	24	16	4	2	1	1	806 ksps	2	5	2	16	31	X	–	–	–
	CY8C4124LQI-S432	24	16	4	2	1	1	806 ksps	2	5	2	16	27	–	X	–	–
	CY8C4124LQI-S433	24	16	4	2	1	1	806 ksps	2	5	2	16	34	–	–	X	–
	CY8C4124AZI-S433	24	16	4	2	1	1	806 ksps	2	5	2	16	36	–	–	–	X
4125	CY8C4125FNI-S423	24	32	4	2	0	1	806 ksps	2	5	2	16	31	X	–	–	–
	CY8C4125LQI-S422	24	32	4	2	0	1	806 ksps	2	5	2	16	27	–	X	–	–
	CY8C4125LQI-S423	24	32	4	2	0	1	806 ksps	2	5	2	16	34	–	–	X	–
	CY8C4125AZI-S423	24	32	4	2	0	1	806 ksps	2	5	2	16	36	–	–	–	X
	CY8C4125FNI-S413	24	32	4	2	1	0	–	2	5	2	16	31	X	–	–	–
	CY8C4125LQI-S412	24	32	4	2	1	0	–	2	5	2	16	27	–	X	–	–
	CY8C4125LQI-S413	24	32	4	2	1	0	–	2	5	2	16	34	–	–	X	–
	CY8C4125AZI-S413	24	32	4	2	1	0	–	2	5	2	16	36	–	–	–	X
	CY8C4125FNI-S433	24	32	4	2	1	1	806 ksps	2	5	2	16	31	X	–	–	–
	CY8C4125LQI-S432	24	32	4	2	1	1	806 ksps	2	5	2	16	27	–	X	–	–
	CY8C4125LQI-S433	24	32	4	2	1	1	806 ksps	2	5	2	16	34	–	–	X	–
	CY8C4125AZI-S433	24	32	4	2	1	1	806 ksps	2	5	2	16	36	–	–	–	X
4146	CY8C4146FNI-S423	48	64	8	2	0	1	1 Msps	2	5	3	16	31	X	–	–	–
	CY8C4146LQI-S422	48	64	8	2	0	1	1 Msps	2	5	3	16	27	–	X	–	–
	CY8C4146LQI-S423	48	64	8	2	0	1	1 Msps	2	5	3	16	34	–	–	X	–
	CY8C4146AZI-S423	48	64	8	2	0	1	1 Msps	2	5	3	16	36	–	–	–	X
	CY8C4146FNI-S433	48	64	8	2	1	1	1 Msps	2	5	3	16	31	X	–	–	–
	CY8C4146LQI-S432	48	64	8	2	1	1	1 Msps	2	5	3	16	27	–	X	–	–
	CY8C4146LQI-S433	48	64	8	2	1	1	1 Msps	2	5	3	16	34	–	–	X	–
	CY8C4146AZI-S433	48	64	8	2	1	1	1 Msps	2	5	3	16	36	–	–	–	X

CY8C			
4		4	PSoC 4
A		0	4000
B	CPU	2	24 MHz
		4	48 MHz
C		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE		AX	TQFP 0.8 mm
		AZ	TQFP 0.5 mm
		LQ	QFN
		PV	SSOP
		FN	CSP
F		I	
S		N/A	PSoC 4A PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ		000-999	

Example



PSoC 4100S 48 TQFP à 40 QFN à 32 QFN ˇ 35 WLCSP Â
ˇ

38.

ID#			DWG
BID20	48 TQFP	7 × 7 × 1.4 mm ˆ ч 0.5 mm˜	51-85135
BID27	40 QFN	6 × 6 × 0.6 mm ˆ ч 0.4 mm˜	001-80659
BID34A	32 QFN	5 X 5 X 0.6 mm ˆ ч 0.45mm˜	001-42168
BID34D	35 WLCSP	TBD	TBD

39.

TA			–40	25	85	°C
TJ			–40	–	100	°C
TJA	θ_{JA}	48 TQFP	–	TBD	–	°C/Watt
TJC	θ_{JC}	48 TQFP	–	TBD	–	°C/Watt
TJA	θ_{JA}	40 QFN	–	TBD	–	°C/Watt
TJC	θ_{JC}	40 QFN	–	TBD	–	°C/Watt
TJA	θ_{JA}	32 QFN	–	TBD	–	°C/Watt
TJC	θ_{JC}	32 QFN	–	TBD	–	°C/Watt
TJA	θ_{JA}	35 WLCSP	–	TBD	–	°C/Watt
TJC	θ_{JC}	35 WLCSP	–	TBD	–	°C/Watt

40.

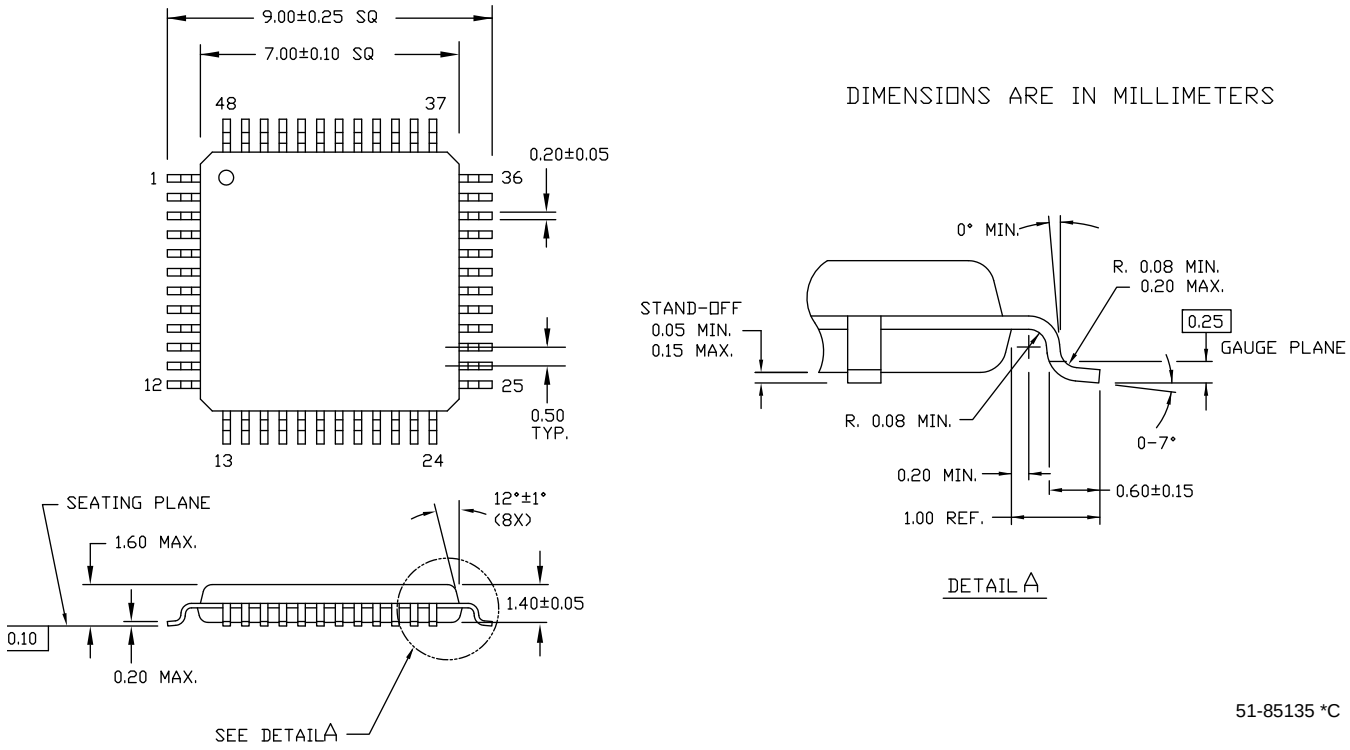
	260 °C	30

41. ˆ MSL˜ IPC/JEDEC J-STD-020

	MSL
	MSL 3

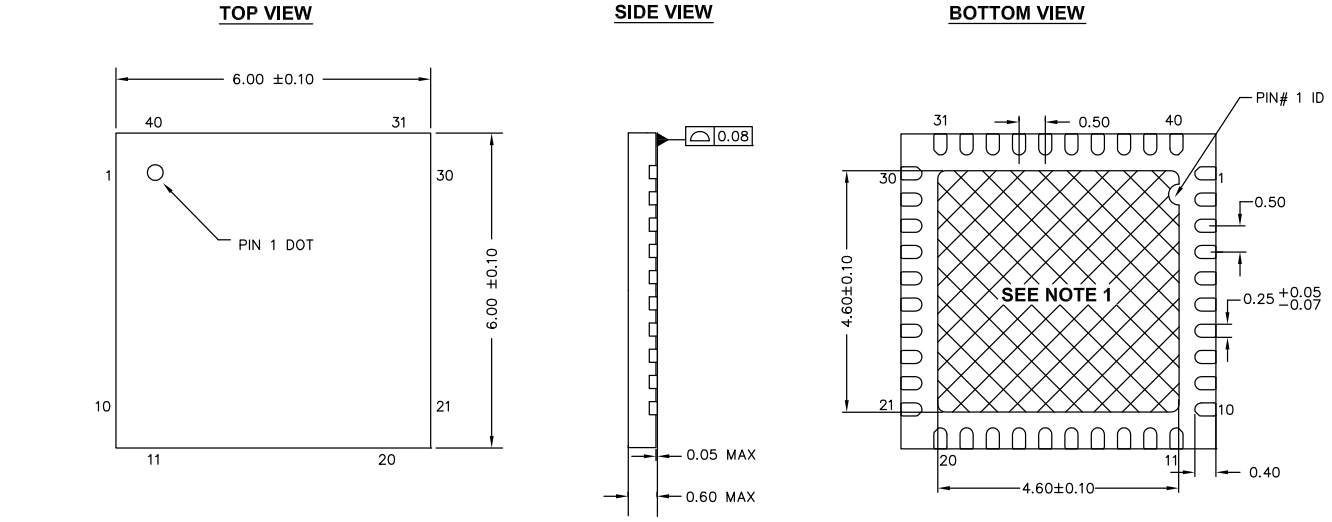
طي

طي 6. 48 TQFP



51-85135 *C

طي 7. 40 QFN

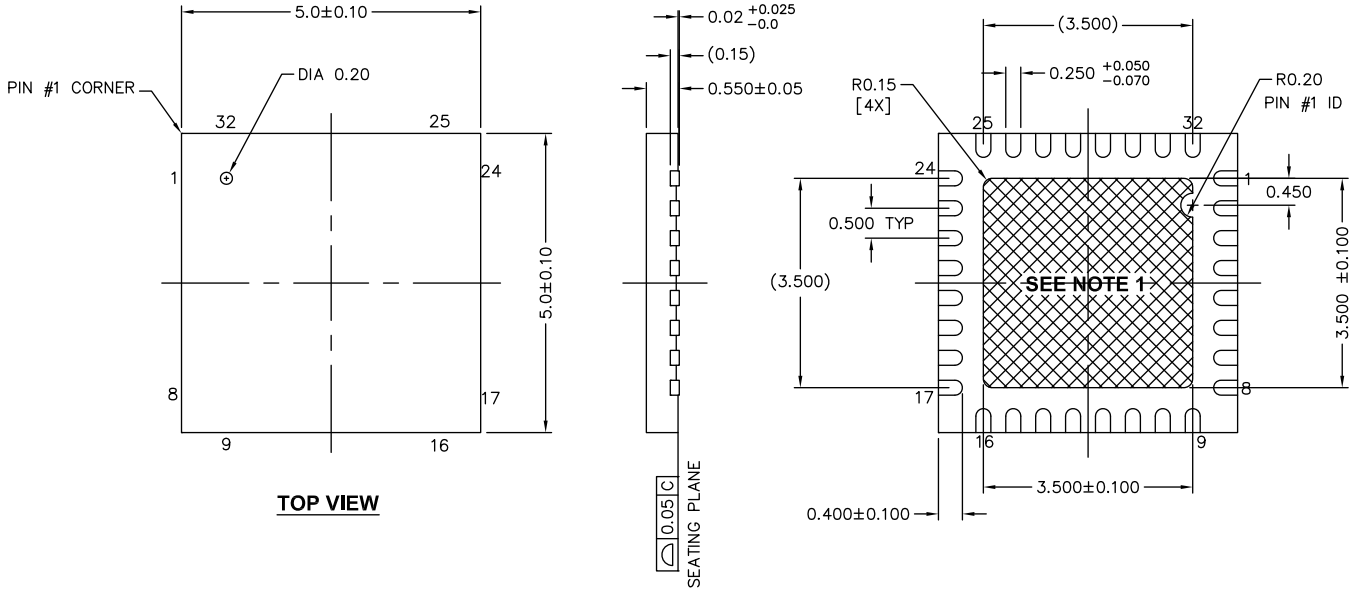


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

ط 8. 32 QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

ط 9. 35 WLCSP

42.

abus	
ADC	
AG	
AHB	AMBA ARM
ALU	
AMUXBUS	
API	
APSR	
ARM®	RISC CPU
ATM	Thump
BW	
CAN	
CMRR	
CPU	
CRC	
DAC	IDAC VDAC
DFB	
DIO	/ GPIO GPIO
DMIPS	Dhrystone
DMA	TD
DNL	INL
DNU	
DR	
DSI	
DWT	
ECC	
ECO	
EEPROM	
EMI	
EMIF	
EOC	
EOF	
EPSR	
ESD	
ETM	
FIR	IIR

42.

FPB	
FS	
GPIO	/ PSoC
HVI	LVI LVD
IC	
IDAC	DAC DAC VDAC
IDE	
I2C IIC	
IIR	FIR
ILO	IMO
IMO	ILO
INL	DNL
I/O	/ GPIO DIO SIO USBIO
IPOR	
IPSR	
IRQ	
ITM	
LCD	
LIN	
LR	
LUT	
LVD	LVI
LVI	HVI
LVTTL	-
MAC	
MCU	
MISO	
NC	
NMI	
NRZ	
NVIC	
NVL	WOL
opamp	
PAL	PLD
PC	
PCB	
PGA	
PHUB	

42. ^ ~

PHY	
PICU	L
PLA	¬
PLD	¬ ^ PAL
PLL	
PMDD	
POR	β
PRES	β
PRS	
PS	Ŋ ^
PSoC®	¬
PSRR	L
PWM	‖ L ^
RAM	Ŋ ^
RISC	Ɔ
RMS	
RTC	
RTL	^
RTR	
RX	
SAR	^
SC/CT	/
SCL	I^2C
SDA	I^2C
S/H	ˇ
SINAD	ˇ
SIO	/ ˇ GPIO Â GPIO Â
SOC	
SOF	
SPI	
SR	
SRAM	Ŋ ^
SRES	β
SWD	
SWV	^
TD	~ DMA
THD	
TIA	^
TRM	

42. ^ ~

TTL	-
TX	
UART	^
UDB	
USB	
USBIO	USB / USB PSoC
VDAC	^ ~ DAC IDAC
WDT	^
WOL	^ ~ NVL
WRES	^ β
XRES	β I/O
XTAL	

β

43. β

	β
°C	
dB	№
fF	
Hz	ĩ
KB	1024
kbps	β
Khr	
kHz	ĩ
kΩ	
ksps	
LSB	β
Mbps	ώ β
MHz	ώ ĩ
MΩ	ώ
Msps	ώ
µA	
µF	
µH	ρ
µs	
µV	
µW	
mA	
ms	
mV	
nA	
ns	
nV	
Ω	
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PSoC® 4 PSoC 4100S 002-10662				
	ECN			
**	5094010	SCHC	02/03/2016	Rev** 002-00122 Rev*C Â

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˜*3K0 ^ ¼AîAÑ _ 1

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